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INTEGRATED CIRCUIT HEATING SYSTEM AND METHOD THEREFOR

Related Patent Documents

This application is related to and fully incorporates U.S. Patent Application Serial No. _____ (AMDA.478PA), entitled "Internal Heating System and Method Therefor," and filed concurrently herewith.

Field of the Invention

The present invention relates generally to semiconductor analysis and, more particularly, to semiconductor analysis involving temperature control of a semiconductor die.

Background of the Invention

The electronics industry continues to rely upon advances in semiconductor technology, including integrated circuits (ICs), to realize higher-functioning devices in more compact areas. For many applications, realizing higher-functioning devices requires integrating a large number of electronic devices into a single silicon die. In addition, many of the individual devices within the die are being manufactured with smaller physical dimensions. As the number of electronic devices per given area of the silicon die increases, and as the size of the individual devices decreases, testing processes become more important and more difficult.

Many integrated circuit dice include circuits having random defects. These defects can recover or fail under particular operating conditions and at higher

temperatures. In addition, design faults can be sensitive to such particular operating conditions. Traditionally, isolation of IC faults has been attempted by operating the die in a manner that causes a failure to occur and by attempting to attribute the failure to a malfunctioning circuit element in the IC. One manner in which this has been performed is to operate the die at full speed while applying external heat to the die. Such electrical testing, however, does not always assist in fault isolation because many failure symptoms can manifest themselves in different ways, and malfunctions can result from a variety of different types of defects including defects at non-suspect circuitry locations.

One such testing application that has traditionally been very difficult to accomplish includes physical diagnosis of failing circuit paths in a semiconductor die. Identifying these "critical circuit paths" has been attempted using simulation in conjunction with a thorough understanding of semiconductor die design, followed by verification using physical probing of a suspect circuit. This physical analysis is difficult, however, because it generally requires intimate knowledge of the die design and is particularly difficult for use in analyzing a flip-chip type integrated circuit die. The identification and analysis of critical circuit paths continues to present a challenge to the advancement of the semiconductor industry.

Summary of the Invention

The present invention is directed to a method and system for analyzing a semiconductor die involving the selective application of heat to the die. The present

invention is exemplified in a number of implementations and applications, some of which are summarized below.

According to an example embodiment, the present invention is directed to a method for analyzing a semiconductor die using a particular application of heat. A region-selective heater having a plurality of heating elements is thermally coupled to the semiconductor die. Various ones of the heating elements are selectively caused to generate heat while the die is operating. The generated heat is used to heat a portion of the die, and a response, such as a failed operation, is detected in connection with analysis of the die. This enhances the ability to identify defects as well as critical circuit paths including, for example, critical timing circuit paths of the semiconductor die; and can be performed without necessarily using expensive laboratory test equipment. In addition, this method does not necessarily require operating the die at a known failing condition or under precisely controlled ambient temperature and voltage conditions.

According to another example embodiment of the present invention, a system is adapted to selectively heat a semiconductor die and to analyze the die in response to the selective heating. The system includes a region-selective heater having a plurality of heating elements and a coupler adapted to couple the heating chip to the die in a manner that makes possible heat transfer from the chip to selected regions of the die. A controller is adapted to activate the heating elements to present heat to selected portions of the die therefrom. The die is operated using a testing device coupled to the die, and a detector is adapted to detect a response from the die.

The above summary of the present invention is not intended to describe each illustrated embodiment or every implementation of the present invention. The figures and detailed description that follow more particularly exemplify these embodiments.

Brief Description of the Drawings

The invention may be more completely understood in consideration of the following detailed description of various embodiments of the invention in connection with the accompanying drawings, in which:

FIG. 1 shows a region-selective die heating system, according to an example embodiment of the present invention; and

FIG. 2 shows an example grid arrangement for use in a region-selective die heating system, according to another example embodiment of the present invention.

While the invention is amenable to various modifications and alternative forms, specifics thereof have been shown by way of example in the drawings and will be described in detail. It should be understood, however, that the intention is not necessarily to limit the invention to the particular embodiments described. On the contrary, the intention is to cover all modifications, equivalents, and alternatives falling within the spirit and scope of the invention as defined by the appended claims.

Detailed Description

The present invention is believed to be applicable for a variety of different types of semiconductor devices, and the invention has been found to be particularly suited for an integrated circuit dice requiring or benefiting from analysis involving the selective

application of heat to the die in order to locally heat a portion of circuitry in the die. While the present invention is not necessarily so limited, aspects of the invention may be appreciated through a discussion of various examples using this context.

According to an example embodiment of the present invention, a heating arrangement is adapted to selectively heat one or more portions of a semiconductor die, such as a wire-bond or flip-chip type die. The heating arrangement includes a region-selective heater that includes a plurality of heating elements. The region-selective heater can be implemented in various arrangements to facilitate selected testing of the die, such as to provide access to the die through the heater, or to couple only to a portion of the die. In one implementation, the heater is provided in a "chip." Other implementations include providing the heater in an adhesive strip, in a semiconductor package substrate, or in any suitable package adaptable to thermally couple to a semiconductor die.

In this particular example embodiment, the region-selective heater is coupled to the die using a common fastener or suitable adhesive. In the case of a flip-chip type die, the heater is coupled to the die over the back side. In the case of a wire-bond die, the heater is placed on a die package, and the die is placed over the heater and bonded to the package via wire-bonds. In one particular implementation, the heater is electrically coupled to the package and operated with an electrical signal provided to the heater via the package. In another particular implementation, the heater is formed in a package to which a wire-bonded die is attached.

Once the heater is coupled to the die, it is connected to an integrated circuit tester and operated to heat selected locations of the die in response to a control input.

The tester applies a test pattern to the die and the die is monitored for any defective operation that would indicate a die malfunction. When defective operation is detected, the corresponding portion of the die being heated is identified as a portion having a suspected defect. Once a portion of the die containing a defect is identified, the die is probed to provide additional defect information.

Various types of defects, such as resistive vias, timing-related defects, defective transistors, short or open circuits and other circuit defects are detectable using the heating arrangement. In the case of detecting timing defects, circuit paths in the die that fail upon operation at high speed or under heat application are often known in view of the design layout. These critical timing paths tend to fail before other portions of the die. The selective addition of heat to the die is used to cause a selected critical timing path to heat, and the increased heat makes the critical timing path more susceptible to failure. When a failure occurs while a particular critical timing path is heated, that failure is an indication that the heated path contains a defect or an improperly designed component of the circuit that fails at higher temperatures. Further analysis is then performed on circuit elements in the critical timing path to better identify the cause of the malfunction.

The integrated circuit tester is adapted to provide multiple test patterns to the die. The test patterns are selected to cause the die to operate in a manner useful for testing purposes. For example, the die can be operated with a normal operation pattern, a preset test pattern, under a high-stress operating condition, or under a test pattern that selectively causes regions of the die to operate. Selectively operating regions of the die is particularly useful for isolating the critical timing paths discussed hereinabove. Input

signals to the die cause circuit elements in a selected critical timing path to operate. Heat is applied to the circuit elements and any defective response is detected and used to identify that one of the circuit elements is suspected of being defective.

In another example embodiment of the present invention, the region-selective heater includes a series of heating elements that are formed in a heating grid. The elements may include, for example, one or more of the following: a transistor, diode, resistive metal trace, polysilicon trace, and a doped substrate area. Such a heating element may include a circuit arrangement having a plurality of semiconductor devices. Each element is coupled to a power supply via interconnects in the heater. When selectively powered, each element generates heat that is used to heat a corresponding portion of the semiconductor die to which the heater is coupled.

In a more particular example embodiment of the present invention, the back side of die is thinned prior to the heater being placed on the back side. Enough substrate is removed from the die to facilitate sufficient heat transfer from the heater to the die. The substrate removal is accomplished using one or more of many removal devices available, employing processes such as CMP, laser etching, FIB and other common processes.

FIG. 1 is a heating system adapted to analyze a semiconductor die, according to another example embodiment of the present invention. A semiconductor die 130 is positioned on a stage 135 and is coupled via the stage to a testing device 140 adapted to generate test signals for the die. Commonly-available testing devices, such as the Teradyne J971, are suitable for stimulating the die. A heater 110 is coupled to the die, and the heater includes a plurality of heater elements adapted to generate heat in

response to being powered. In one implementation, the heater is fastened to the die using a fastener, such as a clamp or other mechanical device, or an adhesive used to fasten the heater to the die. A controller 120 is communicatively coupled to the heater 110 and provides a control signal that causes one or more selected heating elements to operate. The die is operated via the testing device, and a response to the combined heat and operation is detected. The response may, for example, be detected using the testing device itself, or other common laboratory detection devices (*e.g.*, analytical equipment such as an electron beam or laser beam probing system) may be implemented in replacement thereof or in addition thereto. The detected response is then used to analyze the die. Optionally, a computer device 150 is coupled to the controller 120 and/or the testing device 150, and is used to communicate control, response or other data. Response data is provided via the computer for user review.

Once a malfunction of the die has been detected, the portion of the die that is defective or otherwise limited by a design flaw is identified. One example manner in which to identify a defect is to obtain an image of the defective portion of the die, such as a cross-sectional image, and examine the image to identify a particular circuit element that is defective. Another manner is to correlate the location of the heater element causing the defect with a known circuit layout and identify the defective portion of the die therefrom. In another implementation, the computer arrangement is adapted to use the detected response to perform the die analysis, such as by storing or manipulating the response, or by displaying information depicting the particular heater element being operated in order to isolate a critical timing path. The stored or displayed

information can then be compared to empirical data, such as for a properly-functioning die, and variances in the comparison indicate a malfunction.

FIG. 2 shows an example grid arrangement of heater elements, according to another example embodiment of the present invention. The grid may, for example, be implemented in connection with heater 110 of FIG. 1. Each intersection of the grid has a heating element. The elements are referred to by their row (capital letters) and column (numbers) identifications. For example, the element A1 at the circled intersection is identified as such because it is in row A, column 1. The grid elements may include various heat-generating circuitry, such as those elements mentioned hereinabove. In addition, the heater elements can be operated individually, together, in patterns or in virtually any manner consistent with the various applications of the present invention.

In another example embodiment of the present invention, a feedback loop is coupled to one or more of the heating elements. The feedback loop is used to control the action of the heating element. As the temperature changes, the loop is used to provide an indication of the change. This indication is used to detect various aspects of the heat application, such as the temperature, a change in the temperature and a rate of change (increase or decrease) in the temperature. Using the indication supplied by the feedback, the heat application is optimized to meet a desired response. Optimization includes maintaining parameters such as a selected temperature, a selected rate of increase or reduction of heat application and a selected heat differential from one area to another. In addition, the feedback can be used to detect the amount of heat spreading to

surrounding circuitry, and the accuracy of the heat application can be detected therefrom.

In one implementation, the heating element is a transistor having a gate and controlled by way of an electrical bias provided to the gate. In this instance, the feedback loop includes a temperature sensor, such as a temperature sensitive diode, temperature sensitive transistor or a thermocouple. The temperature sensor is coupled to the gate and, as the temperature changes, the sensor applies a bias to the gate that is related to the temperature change. This bias in turn affects the amount of current flowing through the transistor, and thereby regulates the amount of heat generated by the operation of the transistor. For instance, as the temperature increases, the bias applied to the gate via the sensor causes the amount of current flowing through the transistor to decrease, and less heat is generated. Similarly, as the temperature decreases, the bias applied to the gate causes the amount of current flowing through the transistor to increase, and more heat is generated.

In another example embodiment, temperature feedback is used to control the region-selective heater. When the temperature exceeds a selected level, the heater is caused to generate less heat. This is accomplished in different manners, depending upon the application. In one implementation, the heater is operated at a selected operating speed. When the temperature feedback indicates that the amount of heat being supplied is too much, the operating speed is slowed. If more heat is needed, the operating speed is increased. The amount of power supplied to the heater can be altered to control the heat generation in a similar manner.

Monitoring the temperature can be implemented in various ways. In one embodiment, the voltage across an active (transistor) arrangement in a target or representative region in the die is measured at output ports of the heating chip wherein a change in the voltage correlated change in temperature in the target region of the heating chip and/or the die. Depending on the sophistication of the heating chip, the temperature correlation is implemented separate from the die / heating-chip arrangement, *e.g.*, manually or using a computer or calculator, or is implemented using logic and translation devices (such as an analog-to-digital converter for converting the sensed voltage differential to a readable digital temperature code) internal to the heating-chip. Alternatively, the logic and translation devices can be piggy-backed onto the heating-chip and electrically connected to the output ports of the heating chip.

The region-selective heater may be operated in various fashions. In one example embodiment, a control register is formed in the heater, and the control input is effected with the control register. The control register is adapted to selectively activate an individual heating element (such as an arrangement of activatable semiconductor devices) in the heater. The selected element is used to generate heat and thereby heat nearby circuitry in the die. In another example embodiment, the heater is adapted to receive signals from an external control. The external control is used to selectively activate one or more individual heating elements in the heater, and is accomplished either using the control element or by directly activating the heating element. In one implementation, the control input includes a serial signal. Decoding and lookup blocks in the heater interpret the signal and activate one or more heating elements based on the interpreted signal. In another implementation, the external control includes an

activation grid that is electrically coupled to various heater elements in the heater. Selected portions of the grid are activated and corresponding elements in the heater are powered, thereby generating heat. In still another implementation, the activation of the heater elements is pulsed and generates pulses of heat.

The grid operation characteristics are tailored differently to optimize particular testing applications. Various temperature selections and gradients can be used to effect selected tests. In one implementation, the control input is selected to operate various portions of the heater in a sequence. For example, one element can be activated while the remaining elements are left inactive. This provides the ability to selectively heat a small portion of the die being analyzed. In another application, the elements of the heater are heated in a selected sequence. Response data from the die is obtained and recorded relative to the sequence in which the heat is applied.

In another application, heat is applied to a group of elements at a time. A group consisting of adjacent heating elements is selected when it is desired to apply more heat than a single element can provide. This is particularly useful in combination with a feedback loop when a selected temperature is to be maintained. For example, referring to FIG. 2 and using the identification scheme discussed hereinabove, heating elements at locations B1-B4 and C1-C4 are powered, and the die to which the heater is attached begins to heat. If the heating rate is to be increased, additional heating elements at locations A1-A4 and D1-D4 are powered. If the heating rate is to be decreased, heating elements at locations B1-B2 and C1-C2 are shut off. In this manner, the amount of localized heating is readily controlled. Various other combinations are readily available based upon the desired results.

In still another application, and referring again to FIG. 2, the even-numbered elements at locations in rows A, C and E are selectively heated. Selecting elements that are distanced as such caused localized heating in various portions of the die at once, and the distance between the heated elements can be maintained such that heat from each element does not interfere with heat from another element. This is particularly useful, for example, for analyzing groups of critical paths to more efficiently identify defects and to speed the analysis process. If the entire group of critical paths withstand the application of heat via the grid, the heated elements are turned off, another group of elements is powered (*e.g.*, the odd-numbered elements at locations in rows B, D and F), and the test is repeated. Once a defect has been found to exist corresponding to a critical timing path heated by the group of elements, further analysis is performed on portion of the die heated by the group of elements causing a defect.

While the present invention has been described with reference to several particular example embodiments, those skilled in the art will recognize that many changes may be made thereto without departing from the spirit and scope of the present invention, which is set forth in the following claims.